**SYSTEM DESIGN THROUGH VERILOG**

**Assignment-1**

1. Define the following terms relevant to verilog HDL
2. Operators b) Identifiers c) Strengths d) Data types e) System tasks
3. a) Explain in brief built-in-primitives gates that are available in verilog

b) Write a verilog code and test bench for an AOI gate

c) Draw the Half adder circuit in terms of **Ex-OR** gates and **AND** gates. Prepare a Half adder module in terms of **Ex-OR** gate and **AND** gate primitive.

1. a) Design module and a test bench for a half-adder

b)Write a verilog code and test bench for a 4 x 1 mux.

c)Write a verilog code and test bench for an 4 to 16 decoder.

1. a) Write verilog code of an 8-bit counter

b) Describe the behaviour of a JK flip flop using **always** statement

1. a) Write the difference between **begin-end** and **fork-join** blocks with an example

b)Write a verilog code and test bench for 2 to 4 demux using an **if-else construct**

1. a)Write a verilog code and test bench for a D latch in behavioural modeling

b) Write a verilog code and test bench for an addition of two BCD nibbles in behavioural modeling

**All final year students submit the Assignment-1 on or before 20-10-2021(Wednesday) through offline (Hard copy)**